89. The method of claim 81, wherein the chunk of user data is stored in a cache memory prior to being programmed into memory cells within the array.

90. The method of claim 81, wherein the appropriate voltage conditions are applied to said plurality of memory cells in successive applications of voltage pulses that individually shift the threshold level of the cells to which the voltage pulses are applied less than one half of a total change in threshold voltage that is being made.

91. The method of any one of claims 81-90, carried out on a single integrated circuit chip.

A8

92. The method of either of claims 84 or 85, wherein terminating the application of appropriate voltage conditions to individual ones of the plurality of memory cells occurs upon their being determined to have been programmed to within the desired threshold levels by a margin from the breakpoint threshold level.

93. The method of any one of claims 81, 82 or 84, wherein individual ones of the plurality of memory cells are determined to have reached their desired threshold level ranges by comparison with at least one reference level stored in at least one of the memory cells.

94. The method of any one of claims 81, 83 or 85, wherein individual ones of the plurality of memory cells are determined to have reached their desired threshold level ranges by comparison with two or more reference levels stored in two or more of the memory cells.--

REMARKS

The present application, at page 11, lines 27-31, incorporates by reference another application entitled "Multi-State EEprom Read and Write Circuits and Techniques", filed on the same day as the initial parent to the present application, namely April 13, 1989, by Sanjay Mehrotra and Eliyahou Harari, two of the inventors who are also named in the present application. This incorporated application is Serial No. 07/337,579, now abandoned, continuations-in-part of which have issued as patents nos. 5,163,021 and 5,172,338. The present amendment inserts a majority of the incorporated Serial No. 07/337,579 into the present application in order to support claims based thereon that are also being added by this Preliminary Amendment.

Therefore, essentially all of the Summary of the Invention, Brief Description of the Drawings and Description of the Preferred Embodiments sections of Serial No.

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07/337,579 are being added to the present application. In the course of doing so, the patent numbers for referenced applications have also been added. A major revision that has been made to this added text is a change in the drawing figure numbers. Figures 1-17 of Serial No. 07/337,579 are being renumbered herein as figures 9-25, respectively, in order not to use any of the same figure numbers previously used in the present application. Tables 1 and 2 of the incorporated application have also been relabeled as figures 26 and 27, respectively. Further, the reference numbers of the drawings have been changed by adding 1000 to the reference numbers of the figures being incorporated from Serial No. 07,337,579, in order to avoid duplicating the reference numbers already used in the original figures of the present application. Corresponding changes have been made to the text of Serial No. 07/337,579 that is being inserted into the present application.

In addition to providing the attached details showing the changes being made to three paragraphs of the specification (the remainder of this Amendment adds additional material rather than changing the original text), a red-lined copy of the original 1989 parent application is also being filed herewith in order to clearly show all the changes being made by this Amendment. If a copy of the complete application with all the changes of this Amendment is desired without the red-lined markings, the undersigned can promptly provide one upon request.

The claims being substituted into this application are directed to programming memory cells by individually verifying when they have reached their desired programmed states. System claims 27-34, 40-42 and 44 of U.S. patent no. 5,172,338 are directed to similar subject matter with a different scope. Patent no. 5,172,338 was the subject of two reexaminations that were consolidated and which resulted in Reexamination Certificate B1 5,172,338, issued July 8, 1997. The claims of U.S. patent no. 5,991,517 are also directed to similar subject matter with a different scope.

A prompt examination and allowance of the present continuation application is solicited.

EXPRESS MAIL LABEL NO:

EL707909656US

Respectfully submitted,

Gerald P. Parsons, Reg. No. 24,486

May 29, 2001
Date

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DETAILS OF CHANGES TO THE SPECIFICATION TEXT

Page 11, line 23 - page 12, line 5:

Optimized erase implementations have been disclosed in two copending U.S. patent applications. They are copending U.S. patent applications, Serial No. 204,175, filed June 8, 1988, by Dr. Eliyahou Harari, now patent no. 5,095,344, and one entitled "Multi-State EEprom Read and Write Circuits and Techniques," [filed on the same day as the present application] Serial No. 07/337,579, filed April 13, 1989, now abandoned, by Sanjay Mehrotra and Dr. Eliyahou Harari. The disclosures of the two applications are hereby incorporate by reference. The Flash EEprom cells are erased by applying a pulse of erasing voltage followed by a read to verify if the cells are erased to the "erased" state. If not, further pulsing and verifying are repeated until the cells are verified to be erased. By erasing in this controlled manner, the cells are not subject to over-erasure which tends to age the EEprom device prematurely as well as make the cells harder to program.

Page 22, lines 8 - 23:

After the bytes for a write cycle have been loaded into the selected memory device, the controller issues a program command to the memory device and initiate a write cycle. Optimized implementations of write operation for Flash EEprom device have been disclosed in two previously cited co-pending U.S. patent applications, Serial No. 204,175, now patent no. 5,095,344, and one entitled "Multi-State EEprom Read and Write Circuits and Techniques," Serial No. 07/337,579, filed April 13, 1989, now abandoned. Relevant portions of the disclosures are hereby incorporated by reference. Briefly, during the write cycle, the controller applies a pulse of programming (or writing) voltages. This is followed by a verify read to determine if all the bits have been programmed properly. If the bits did not verify, the controller repeats the program/verify cycle until all bits are correctly programmed.

Page 25, line 32 - page 26, line 11:

In the present invention, a system of Flash EEprom is used to provide non-volatile memory in place of traditional system memories such as disk storage. However, Flash EEprom memory is subject to wearing out by excessive program/erase cycles. Even with the improved Flash EEprom memory device as disclosed in co-pending U.S. patent applications, Serial No. 204,175, now patent no. 5,095,344, and one entitled "Multi-state

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EEprom Read and Write Circuits and Techniques," by Sanjay Mehrotra and Dr. Eliyahou Harari, Serial No. 07/337,579, filed April 13, 1989, now abandoned, [filed on the same day as the present application,] the endurance limit is approximately 10^6 program/erase cycles. In a ten-year projected life time of the device, this translates to a limit of one program/erase cycle per 5 minutes. This may be marginal in normal computer usage.

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